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Harold C. Moore
Name of person mailing Document or Fee

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November 7, 2006
Date of Signature

Re:	Application of:	Kahlisch et al.
	Serial No.:	10/719,999
	Filed:	November 21, 2003
	For:	Supporting Structure for a Chip and Method for Producing the Same
	Group Art Unit:	2814
	Confirmation No.:	1506
	Examiner:	Shrinivas H. Rao
	Our Docket No.:	1890-0011

TRANSMITTAL OF BRIEF ON APPEAL

Please find for filing in connection with the above patent application the following documents:

1. Appeal Brief;

2. Check in the amount of $500.00; and

3. One (1) return post card.

The Notice of Appeal was received on September 11, 2006, in the U.S. Patent and Trademark Office, and therefore the due date for the Appeal Brief is November 11, 2006 (M.P.E.P. 1205.01). Since the due date for filing the Appeal Brief falls on November 11,, 2006, the Appeal Brief is being timely filed on November 7, 2006.

Enclosed please find a check in the amount of $500.00 to cover the filing fee of a Brief on Appeal as required by 37 C.F.R. § 1.17(c). Please charge any deficiency, or credit any overpayment to Deposit Account No. 13-0014.

Respectfully Submitted,
MAGINOT, MOORE & BECK, LLP

November 7, 2006

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Enclosures

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Sir:

This is an appeal under 37 CFR § 41.31 to the Board of Patent Appeals and Interferences of the United States Patent and Trademark Office from the rejection of claims 1, 3-11, 13, 14 and 23-31 of the above-identified patent application. Claims 1, 3-11, 13, 14 and 23-31 have been finally rejected in an office action dated April 6, 2006. A check in the amount of **$500.00** is enclosed herewith. Also, please provide any extension of time which may be necessary and charge any fees which may be due to Deposit Account No. 13-0014, but not to include any payment of issue fees.

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(1) REAL PARTY IN INTEREST

Infineon Technologies AG is the owner of this patent application, and therefore the real party in interest.

(2) RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences in this case.

(3) STATUS OF CLAIMS

Claims 1, 3-11, 13, 14 and 23-31 are pending in the application.

Claims 1, 3-11, 13, 14 and 23-31 stand rejected and form the subject matter of this appeal. Claims 1, 3-11, 13, 14 and 23-31 are shown in the Appendix attached to this Appeal Brief.

(4) STATUS OF AMENDMENTS

Applicants filed a Response to Office Action dated February 3, 2005 ("First Response") responsive to an Office Action dated November 3, 2004. A final Office Action dated May 5, 2005 was designated by the Examiner to be responsive to the First Response. On August 4, 2005, Applicants filed an RCE and Amendment ("RCE Amendment") that was responsive to the final Office Action. The Examiner thereafter issued another office action dated October 17, 2005 ("Post RCE Office Action") responsive to the RCE Amendment. Applicants filed a Response to Office Action ("Post RCE Response") on January 17, 2006 that was responsive to the Post RCE Office action. The Examiner then issued a final Office

Action dated April 6, 2006 ("Second Final Action"), which was designated to be responsive to the Post RCE Response.

(5) SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1 is directed to an arrangement for use in a package that includes a supporting substrate, an interconnect layer, a chip, at least one wire, an encapsulation material and an escape prevention structure. (See, e.g., the device of Figs. 1A and 1B). The supporting substrate has a bond opening therein. (See, e.g., supporting substrate 100 and bond opening 116 of Figs. 1A and 1B; See also specification at p.10, lines 9-10).

The interconnect layer is disposed on the supporting substrate. (See, e.g., interconnect layer 110 of Figs. 1A and 1B). A bonding channel overlapping with the bond opening is formed in the interconnect layer. (See, e.g., bonding channel 114 of Figs. 1A and 1B, see also specification at p.10, lines 9-11). The chip is fixed to the interconnect layer to cover the bonding channel. (See, e.g., chip 112 of Fig. 1A).

The "at least one" wire is connected to the chip and extends through the bond opening and the bonding channel (See specification at p.9, lines 29-33). The encapsulation material is arranged in the bonding channel. (See *id.* at p.10, lines 9-16). The escape prevention structure is configured to enable escaping of air from the bonding channel and to substantially prevent the encapsulation material from escaping from the bonding channel. (See, e.g. barrier structures 120 of Figs. 1A and 1B; see also specification at p.10, line 28 to p.11, line 6).

Independent claim 23 is also directed to an arrangement for use in a package. The arrangement of claim 23 includes a supporting substrate, an interconnect layer, a chip, an encapsulation material and an escape prevention structure. The supporting substrate has a bond opening therein. (See, e.g., supporting substrate 100 and bond opening 116 of Figs. 1A and 1B; See also specification at p.10, lines 9-10).

The interconnect layer is disposed on the supporting substrate. (See, e.g., interconnect layer 110 of Figs. 1A and 1B). A bonding channel overlapping with the bond opening is formed in the interconnect layer. (See, e.g., bonding channel 114 of Figs. 1A and 1B, see also specification at p.10, lines 9-11). The bond opening and bonding channel are configured to receive at least one bond wire. (See specification at p.9, lines 29-33).

The chip is fixed to the interconnect layer and covers the bonding channel. (See, e.g., chip 112 of Fig. 1A). The encapsulation material is arranged in the bonding channel. (See *id.* at p.10, lines 9-16).

The escape prevention structure is configured to enable escaping of air from the bonding channel and to substantially prevent the encapsulation material from escaping from the bonding channel. (See, e.g. barrier structures 120 of Figs. 1A and 1B; see also specification at p.10, line 28 to p.11, line 6).

(6) ISSUES

Whether claims 1, 3-11, 13 and 14 are unpatentable under 35 U.S.C. § 103(a) as allegedly being obvious over U.S. Patent Publication No. 2002/0090092162, now U.S. Patent No. 6,772,512 to Tsai et al. (hereinafter "Tsai") *or* U.S. Patent No. 4,888,885 to Kovac (hereinafter "Kovac") in view of U.S. Patent No. 5,763,952 to Lynch (hereinafter "Lynch").

Whether claims 23-31 are unpatentable for unspecified reasons.

> supporting structure for a chip, comprising: a supporting substrate with a bond opening therein (Tsai figure 2A # 210 substrate, opening # p, or Kovac figures 2-3 # 10 with opening 16, col. 3, lines 60-67); an interconnect layer on the supporting substrate Tsai figure 2 B # 221, or Kovac figure 4 # 12) in which a bonding channel overlapping with the bond opening is formed, (Tsai figure 2B-C, # 211 etc. or Kovac col. 4, lines 4-6, not illustrated in figures) and a chip fixed to the interconnect layer to cover the bonding channel (Tsai figure 2 B 220).

(Second Final Action at p.3). As an initial manner, the Examiner has alleged that the claimed *interconnect layer* is element 12 of Kovac. Element 12 of Kovac is a cover plate 12 of a fixture 10. The fixture 10 of Kovac is a fixture in which a workpiece is temporarily placed. (See generally Kovac at col. 3 line 58 to col. 4, line 15).

Thus to satisfy claim 1, the bonding channel of Kovac *must* be in the cover plate 12 of the fixture 10, because the claimed bonding channel is formed in the *interconnect layer*. The Examiner, however, admits that Kovac does not *show* the claimed bonding channel in the figures. (Second Final Action at p.3). Nevertheless, the Examiner alleges that the text of Kovac does teach a bonding channel. (*Id.*)

In particular, the Examiner cites the teaching of a bonding channel in Kovac at column 4, lines 4-6. (See Second Final Action at p.3). The cited passages read "[The openings] 20, as illustrated in FIG. 3 are all coupled to a common manifold 22 channeled in the block 10 which recess air from an air source, not illustrated." (Kovac at col. 4, lines 3-6). This portion of Kovac appears to teach two different structures that could potentially be considered to be channels: the openings 20 and the common manifold 22. Both elements constitute a channel of sorts, and both are admittedly located within the cover plate 12.

However, the openings 20 and manifold 22 of Kovac do not contain and would never contain "encapsulation material", as is required of the bonding channel of claim 1. Kovac very clearly discloses that the openings 20 and manifold 22 are provided in the fixture 10 to provide air flow to a workpiece that is disposed on the fixture 10. (*Id.*) Kovac does not teach or suggest that those openings ever include an encapsulation material. Indeed, the air flow

openings 20 and manifold 22 would never include encapsulation material because it would restrict or prevent the intended purpose of those structures – to provide air flow.

There does not appear to be any other channel in the cover plate 12 of the fixture. Accordingly, based on the Examiner's characterization of the cover plate 12 of Kovac as the interconnect layer, Kovac fails to disclose or suggest a bonding channel that includes encapsulation material, where the bonding channel is disposed in the interconnect layer.

Moreover, the Examiner never alleges a modification of Kovac to include such a channel in an interconnect layer (i.e. the cover plate 12) where an encapsulating material is arranged in the bonding channel. Instead, the only modification that the Examiner only alleges is that it would have been obvious "to include Lynch's at least one wire connected to the chip and extending through the bond opening and the bonding channel in Kovac's device". (Second Final Action at p.3). Even if this modification were made to Kovac, the resulting structure would still lack an encapsulating material in the channel of the cover plate 12.

As a consequence, the Examiner has not alleged a combination of Kovac and Lynch that arrives at the invention of claim 1. For at least this reason, it is respectfully submitted that the rejection of claim 1 over Kovac and Lynch is in error and should be reversed.

2. No Motivation to Place Wire in Channels of Cover Plate 12 of Kovac

In addition, there is no motivation or suggestion to modify Kovac as proposed by the Examiner. As discussed above, the Examiner has alleged that the claimed interconnect layer is satisfied by the cover plate 12 of the fixture 10 of Kovac. (See Second Final Action at p.2) As further discussed above, to the extent the cover plate 12 of Kovac has *any* channels that

could constitute the claimed "bonding channels", those channels are the openings 20 and/or channels 22. (See, e.g., Kovac at Fig. 3). Those openings and channels 20 and 22, however, only move air to and from the workpiece. (See *id.* at cols. 3 and 4).

The Examiner's proposed combination is to "include Lynch's at least one wire connected to the chip and extending through the bond opening and the bonding channel in Kovac's device" (Second Final Action at p. 3). Thus, the Examiner proposes placing a wire in the opening 20 or channel 22 of the cover plate 12 of Kovac. The motivation provided by the Examiner is to "form well supported leads ... and selected external portions of the selected lead traces can be connected to ground or power and the beneficial electrical characteristics discussed above accrue to a flexible, tape mounted semiconductor assembly". (Second Final Action at pp.3-4).

It is submitted that the Examiner's motivation is legally insufficient. In particular, placing leads in the air channels 20, 22 of the cover plate 12 of Kovac would not result in the formation of "well supported leads". The leads would be placed, apparently temporarily, within air channels of a fixture. Once the substrate is removed from the Kovac fixture, the leads would not be "well supported" by anything. Moreover, Lynch does *not* in any way suggest placing wire leads, in the air vents of a workpiece fixture. Thus, Lynch does not suggest placing wire leads in the air channels 20, 22 of the fixture 10 of Kovac.

Thus, in addition to the fact that the proposed combination does not arrive at the invention, there is no motivation or suggestion to make the proposed combination.

For either or both of these reasons, the rejection of claim 1 over Kovac and Lynch is in error and should be withdrawn.

C. The Rejection of Claim 1 Over Tsai and Lynch

The Examiner has not alleged *any* modification of Tsai that would arrive at the invention of claim 1. In particular, the Examiner admits the Tsai fails to teach "at least one wire connected to the chip and extending through the bond opening and the bonding channel". (Second Final Action at p.3). The Examiner, however, never alleges *any* modification of Tsai that would include the claimed wire extending through the bond opening. (*Id.*) A prima facie case of obviousness requires, as a threshold matter, a proposed modification that arrives at the claimed invention. The Examiner has proposed no such modification.

While the Examiner alleges a modification of Kovac in view of Lynch, the Examiner does not identify any modification of Tsai in view of Lynch that arrives at the invention of claim 1.

Accordingly, the Examiner has failed to allege a prima facie case of obviousness of claim 1 over Tsai and Lynch. For at least this reason, the rejection of claim 1 over Tsai and Lynch should be reversed.

D. The Rejection of Claims 3-11, 13 and 14

Claims 3-11, 13 and 14 all stand rejected as allegedly being obvious over Tsai or Kovac in view of Lynch. Claims 3-11, 13 and 14 all depend from and incorporate all of the limitations of claim 1. Accordingly, for at least the same reasons as those discussed above in connection with claim 1, it is respectfully submitted that the rejections of claims 3-11, 13 and 14 are in error and should be reversed.

II. The Obviousness Rejection of Claims 23-31

The Examiner has not specifically alleged any rejection of claim 23. (See Second Final Action, pp.2-9). However, it appears that the Examiner intended to reject claim 23 as obvious over either Tsai or Kovac in view of Lynch, using the same reasoning as that applied to claim 1. As discussed above, the Examiner has not set forth a prima facie case of obviousness with respect to claim 1. For substantially the same reasons as those set forth above in connection with claim 1, it is submitted that the rejection of claim 23 should be reversed.

Claims 24-31 depend from and incorporate all of the limitations of claim 23. Accordingly, for at least the same reasons as those set forth above in connection with claim 23, the rejection of claims 24-31 over Tsai or Kovac in view of Lynch should be reversed.

(8) CONCLUSION

For all of the foregoing reasons, claims 1, 3-11, 13, 14 and 23-31 are not unpatentable under 35 U.S.C. § 103(a). As a consequence, the Board of Appeals is respectfully requested to reverse the rejection of these claims.

Respectfully submitted,

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CLAIM APPENDIX

Claim 1. An arrangement for use in a package, comprising:

a supporting substrate with a bond opening therein;

an interconnect layer on the supporting substrate, in which a bonding channel overlapping with the bond opening is formed;

a chip fixed to the interconnect layer to cover the bonding channel;

at least one wire connected to the chip and extending through the bond opening and the bonding channel;

an encapsulation material arranged in the bonding channel; and

an escape prevention structure for the bonding channel, to enable escaping of air from the bonding channel and to substantially prevent the encapsulation material from escaping from the bonding channel.

Claim 2. The arrangement of claim 1, wherein the escape prevention structure is designed to prevent escaping of the encapsulation material due to the capillary effect.

Claim 3. The arrangement of claim 1, wherein the escape prevention structure includes an opening with such a cross-sectional area, so that escaping of the encapsulation material caused by the capillary effect is prevented.

Claim 4. The arrangement of claim 1, wherein the bonding channel is open at a lateral end, wherein the escape prevention structure is formed at the lateral end by a barrier structure for reducing a cross-section of the bonding channel at the lateral end.

Claim 5. The arrangement of claim 4, wherein the barrier structure is connected to the interconnect layer.

Claim 6. The arrangement of claim 4, wherein the barrier structure is formed integrally with the interconnect layer.

Claim 7. The arrangement of claim 4, wherein the barrier structure extends across the entire width of the bonding channel.

Claim 8. The arrangement of claim 4, wherein the barrier structure is formed, so that a cross-section of the bonding channel tapers in a direction to the lateral end.

Claim 9. The arrangement of claim 4, wherein the barrier structure has a convex shape.

Claim 10. The arrangement of claim 4, wherein the barrier structure is disposed in the bonding channel and spaced from the interconnect layer.

Claim 11. The arrangement of claim 1, wherein the escape prevention structure includes a recess in the supporting substrate.

Claim 13. The arrangement of claim 11, wherein the interconnect layer is disposed on a surface of the supporting substrate, wherein the recess on the surface extends across a sidewall of the bonding channel.

Claim 14. The arrangement of claim 11, wherein the recess is disposed in a region of the bonding channel, wherein the recess extends from a first surface of the supporting substrate to a second surface of the supporting substrate.

Claim 23. An arrangement for use in a package, comprising:

a supporting substrate with a bond opening therein;

an interconnect layer disposed on the supporting substrate;

a bonding channel overlapping with the bond opening disposed in the interconnect layer, said bond opening and bonding channel configured to receive at least one bond wire;

a chip fixedly secured to the interconnect layer and substantially covering the bonding channel;

an encapsulation material arranged in the bonding channel; and

an escape prevention structure disposed between the chip and the supporting substrate, the escape prevention structure configured to substantially prevent an encapsulation material flow out of the bonding channel, and further configured to enable escaping of air from the bonding channel.

Claim 24. The arrangement of claim 23, wherein the bonding channel has an opening at a lateral end, and wherein the escape prevention structure defines the cross section of the opening of the bonding channel.

Claim 25. The arrangement of claim 24, wherein the escape prevention structure includes a portion connected to the interconnect layer.

Claim 26. The arrangement of claim 24, wherein the escape prevention structure includes a portion formed integrally with the interconnect layer.

Claim 27. The arrangement of claim 24, wherein the escape prevention structure includes a portion that extends across the entire width of the bonding channel.

Claim 28. The arrangement of claim 24, wherein the escape prevention structure is formed such that a cross-section of the bonding channel tapers in a direction to the lateral end.

Claim 29. The arrangement of claim 24, wherein the escape prevention structure has a convex shape.

Claim 30. The arrangement of claim 24, wherein the escape prevention structure is disposed in the bonding channel and spaced from the interconnect layer.

Claim 31. The arrangement of claim 24, wherein the escape prevention structure includes a recess in the supporting substrate.

EVIDENCE APPENDIX

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[NONE]

RELATED PROCEEDINGS APPENDIX

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[NONE]